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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/522,085

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Antonius Adrianus Maria Van Wel

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EXAMINER

ELLIS, KEVIN L

ART UNIT

PAPER NUMBER

2188

DATE MAILED: 07/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/522,085

Applicant(s)

VAN WEL, ANTONIUS ADRIANUS
MARIA

Examiner

Kevin L. Ellis

Art Unit

2188

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 26 May 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-8 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-8 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

Detailed Action

1. Claims 1-8 are presented for examination.

Claim Rejections – 35 USC § 101

2. In claim 8, Applicant sets forth a "computer program comprising computer program means for instructing a computer system". This claim language does not tangibly embody a computer program stored on a computer readable medium. Therefore, the claim language used does not meet the "useful, concrete, and tangible" requirement as set forth in *State Street*, 149 F.3d at 1373, 47 USPQ2d at 1601-02, and hence claim 8 is not statutory under 35 U.S.C. 101.

Claim Rejections – 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(c) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

4. Claims 1-8 are rejected under 35 U.S.C. § 102(b) as being anticipated by Sakakibara et al., U.S. Patent 5,590,353.

A) As to claims 1 and 4, Sakakibara et al. discloses the invention as claimed. There is a method for transmitting a vector in a computer system comprising a processor (see Fig

1), a multi-port memory (Fig 1 Ref 220), passing a base memory address to an address configuration means (see Col 1 Lines 13-56 and Col 15 Line 15 to Col 16 Line 55; specifically Fig 5 Ref 191-1, see Col 15 Lines 30-65), defining a set of memory addresses by the address configuration means using the base memory address and a configuration instruction for configuring the address configuration means (see Col 15 Line 15 to Col 16 Line 55), transmitting the vector to/from the multi-port memory using the set of memory addresses (see Col 15 Line 15 to Col 16 Line 55).

- B) As to claims 2 and 5, the address configuration means does include a plurality of register files (see Fig 1 Ref 191, 192, 193, and 194).
- C) As to claims 3 and 6, the configuration does include an offset (see Col 15 Line 30 to Col 16 Line 23).
- D) As to claim 7, the multi-port memory and the address configuration means can be considered to be included in a "memory system" (see Fig 1).
- E) As to claim 8, the limitations have been addressed with respect to claim 1 above. As for the computer program it is inherent that a "program" would be executed by Sakakibara et al. that would cause the addresses to be created that are provided to the multi-port memory.

5. Claims 1, 2, 4, 5, 7, and 8 are rejected under 35 U.S.C. § 102(b) as being anticipated by Duboc, U.S. Patent 6,463,518.

- A) As to claims 1 and 4, Duboc discloses the invention as claimed. There is a method for transmitting a vector in a computer system comprising a processor (see Fig 2 Ref 12),

a multi-port memory (Fig 2 Ref 14), passing a base memory address to an address configuration means (Fig 2 Ref 40 and Col 8 Lines 32-42), defining a set of memory addresses by the address configuration means using the base memory address and a configuration instruction for configuring the address configuration means (see Fig 4 and Col 8 Line 42 to Col 9 Line 65), transmitting the vector to/from the multi-port memory using the set of memory addresses (see Col 6 Line 63 to Col 7 Line 43).

- B) As to claims 2 and 5, the address configuration means does include a plurality of register files (see Fig 4).
- C) As to claim 7, the multi-port memory and the address configuration means can be considered to be included in a "memory system" (see Fig 2).
- D) As to claim 8, the limitations have been addressed with respect to claim 1 above. As for the computer program it is inherent that a "program" would be executed by Duboc that would cause the addresses to be created that are provided to the multi-port memory.

Response to Arguments

6. Applicant's arguments filed 5/25/06 have been fully considered but they are not persuasive.

Applicant argues that with regard to Sakakibara, there "is no base memory address that is used to define a set of memory addresses as in the present invention." (see P 2 ¶ 4 of Amendment). However, Sakakibara et al. does in show a base memory address that is used to define a set of memory addresses as claimed by the present invention. As discussed at column 15 line 15 to column 16 line 55, the base memory address is used to define a set of memory addresses that are used to transmit the vector to/from the memory. A single base address is used

to define a set of memory addresses. The fact that the system of Sakakibara et al. also has multiple access request control units, each using a base memory address and each base memory address being used to create a different set of memory addresses does not preclude it from reading upon the claimed invention. In addition, the claim uses the word "comprising" so addition elements can be present. Applicant makes similar arguments with regard to Duboc, but is not found persuasive for the same reasons.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin L. Ellis whose telephone number is 571-272-4205. The examiner can normally be reached on weekdays from 6:00AM-2:30PM.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 571-272-4210. The fax phone numbers for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Kevin L. Ellis
Primary Examiner
July 26, 2006

